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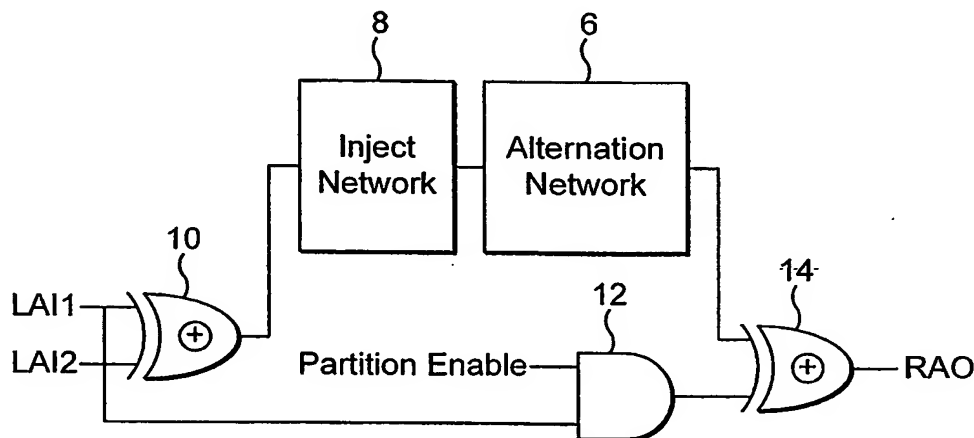
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(54) Title: **SCALABLE PROCESSING NETWORK FOR SEARCHING AND ADDING IN A CONTENT ADDRESSABLE MEMORY**



(57) **Abstract:** An alternation network for use with a content addressable memory for implementing a divide and conquer algorithm is described. The alternation network comprises: a plurality of alternation modules connected in series together, each module comprising: a plurality of cascaded logic gates arranged to propagate a match parity signal via the gates along at least part of a matching result vector, the matching result vector being generated by execution of a matching instruction on the content addressable memory, and the logic gates being configured to change the parity of the match parity signal in accordance with the matching result vector; and a vector output arranged to output a parity level vector of the propagated match parity signal present at the each gate of the plurality of logic gates; a logic network for dividing the matching result vector into an odd match vector and an even match vector representing respectively odd and even numbered elements of the matching result vector, by use of the parity level vector; and means for writing a selected one of the odd and even match vectors to the content addressable memory.

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